Translation of German Published Non-Prosecuted Patent Application DE 100 45 694 A1

Description

Semiconductor memory cell with trench capacitor and selection transistor and method for fabricating it.

The present invention relates to a semiconductor memory cell having a trench capacitor and a selection transistor, and to a method for fabricating it.

Integrated circuits (ICs) or chips use capacitors for the purpose of storing charge, such as e.g. a dynamic random access memory (DRAM). The charge state in the capacitor represents a data bit in this case.

A DRAM chip contains a matrix of memory cells which are arranged in the form of rows and columns and are driven by word lines and bit lines. The reading of data from the memory cells or the writing of data to the memory cells is realized by activating suitable word lines and bit lines.

A DRAM memory cell usually contains a transistor connected to a capacitor. The transistor contains two diffusion regions which are separated from one another by a channel controlled by a gate. Depending on the direction of the current flow, one diffusion region is referred to as the drain and the other as the source. The drain region is connected to the bit line, the source region is connected to the trench capacitor and the gate is connected to the word line. By applying suitable voltages to the gate, the transistor is controlled in such a way that a current flow between the drain region and the source region through the channel is switched on and off.

The charge stored in the capacitor decreases over time on account of leakage current. Before the charge has decreased to an indeterminate level below a threshold value, the capacitor must be refreshed. For this reason, these memory cells are referred to as dynamic RAM (DRAM). A typical configuration of a semiconductor memory having a trench capacitor and a selection transistor is specified in the patent specification US 5,867,420.

One problem in known DRAM variants is the production of a sufficiently large capacitance for the trench capacitor. This problem will be aggravated in future by the advancing miniaturization of semiconductor components. The continuous increase in the integration density means that the area available per memory cell and thus the capacitance of the trench capacitor decrease ever further. An excessively low capacitance of the trench capacitor can adversely affect the functionality and useability of the memory device since an excessively small quantity of charge is stored in the trench capacitor.

By way of example, sense amplifiers require a sufficient signal level for reliably reading out the information situated in the memory cell. The ratio of the storage capacitance of the trench capacitor to the bit line capacitance is crucial in determining the signal level. If the storage capacitance of the trench capacitor is too low, said ratio may be too small for generating an adequate signal in the sense amplifier.

A low storage capacitance likewise requires a higher refresh frequency, because the quantity of charge stored in the trench capacitor is limited by its capacitance and additionally decreases due to leakage currents. If the quantity of charge falls below a minimum quantity of charge in the storage

capacitor, then it is no longer possible for the information stored therein to be read out by the connected sense amplifiers, the information is lost and read errors arise.

One way of avoiding read errors is to reduce the leakage currents. Leakage currents can be reduced on the one hand by transistors and on the other hand by dielectrics, such as e.g. the capacitor dielectric. An undesirably reduced retention time can be lengthened by these measures.

A trench capacitor is usually used in DRAMS. A trench capacitor has a three-dimensional structure which is formed in a silicon substrate. An increase in the trench capacitor electrode area and thus in the capacitance of the trench capacitor can be achieved by etching more deeply into the substrate. In this case, the increase in the capacitance of the trench capacitor does not cause the substrate surface occupied by the memory cell to be enlarged. However, this method is limited since the attainable etching depth of the trench capacitor depends on the trench diameter, and, during fabrication, it is only possible to attain specific finite aspect ratios (ratio between trench depth and trench diameter).

As the increase in the integration density advances, the substrate surface available per memory cell decreases ever further. The associated reduction in the trench diameter inevitably leads to a reduction in the capacitance of the trench capacitor. If the capacitance of the trench capacitor is dimensioned to be so low that the charge which can be stored is insufficient for entirely satisfactory read-out by the sense amplifiers connected downstream, then this results in read errors.

The patent specification US 5,360,758 discloses that, in memory cells with trench capacitor and selection transistor, it is necessary to comply with a minimum distance between the trench capacitor and the transistor. This is necessary since, during thermal steps, the electrical contact between the trench capacitor and the transistor is produced by the outdiffusion of dopant originally situated in the trench capacitor. In this case, the outdiffusion of the dopant typically extends over distances of between 50 and 150 nanometers (nm). It must be ensured in this case that the dopant does not diffuse into the channel of selection transistor, where it can lead to increased leakage currents through the transistor which render the relevant memory cell unusable. This means that a memory cell that is theoretically possible without outdiffusion has to be enlarged by the size of the outdiffusion.

The object of the invention is to specify a semiconductor memory cell with reduced space requirement and improved retention time, and a method for fabricating it.

The object is achieved by means of a semiconductor memory cell having:

- a trench, in which a trench capacitor is arranged;
  a selection transistor, which is arranged as a planar transistor above the trench capacitor;
- a capacitor dielectric, which is arranged in the trench;
- a conductive trench filling, which is arranged in the trench;
- a diffusion barrier, which is arranged on the conductive trench filling;
- an epitaxial layer grown epitaxially over the diffusion barrier;

- a source doping region of the selection transistor, which is arranged in the epitaxial layer.

By virtue of the arrangement according to the invention, firstly a diffusion barrier is arranged on the conductive trench filling. The diffusion barrier has the task of preventing an outdiffusion of dopant situated in the conductive trench filling, which might damage the selection transistor. What is novel in this case is that the diffusion barrier is formed horizontally. In order that the space used by the memory cell is made as small as possible, measures are taken to arrange the selection transistor as far as possible directly above the trench capacitor. To that end, the trench capacitor and the diffusion barrier are overgrown with an epitaxial layer. In this case, the epitaxial layer forms in a monocrystalline fashion, so that a source doping region of the selection transistor can be arranged in it.

An arrangement according to the invention provides for the source doping region of the selection transistor to be contact-connected from underneath with the diffusion barrier. Contact-connecting the diffusion region from underneath advantageously enables space to be saved, so that the substrate surface used by the memory cell can be made as small as possible. Furthermore, the direct contact-connection of the source doping region ensures a low-resistance connection between the diffusion barrier and the source doping region.

A further configuration of the invention provides for the diffusion barrier to be arranged horizontally. By virtue of the horizontal arrangement of the diffusion barrier, it is possible, by way of example, to provide the entire trench cross section with the diffusion barrier, with the result that, firstly, the outdiffusion of dopant from the trench is

prevented and, secondly, an area that is as large as possible is contact-connected with the source doping region of the selection transistor, which ensures a low-resistance contact. The diffusion barrier also comprises a vertical contact area. Furthermore, the diffusion barrier between the trench and the source doping region is buried in the source doping region, thereby reducing the pn junction area of the source doping region with respect to the channel and hence the leakage current.

A further variant of the invention provides for an insulating covering layer with an inner hole to be arranged on the conductive trench filling. The insulating covering layer first of all insulates the conductive trench filling from the overlying epitaxial layer grown epitaxially. The inner hole in the covering layer ensures, however, that it is possible to produce an electrical contact between the conductive trench filling and the source doping region - arranged in the epitaxial layer - of the selection transistor. A further variant of the invention provides for a conductive contact to be arranged in the inner hole. The conductive contact is formed in such a way that it makes contact with the conductive trench filling and fills the inner hole of the dielectric layer. By way of example, the conductive trench filling comprises tungsten, tungsten nitride, titanium nitride, arsenic- or phosphorus-doped polysilicon or amorphous silicon.

A further advantageous configuration of the invention provides for the conductive contact to connect the conductive trench filling to the source doping region of the selection transistor. This arrangement produces a conductive contact between the trench capacitor and the selection transistor.

In a further advantageous configuration of the invention, the cross-sectional area of the inner hole in the dielectric layer is smaller than the cross-sectional area of the trench. This configuration ensures that the trench can have a large cross section, and the trench capacitor thus has a large capacitance, even if the selection transistor is made relatively small. As a result, a small source doping region is made possible since the cross-sectional area of the inner hole is made smaller than the cross-sectional area of the trench, which can thus be adapted to the size of the source doping region. The small source doping region additionally has the advantage that the leakage current between channel and source doping region is reduced.

Furthermore, it is provided that the insulating covering layer is formed as a lateral edge web. Forming the insulating covering layer as a lateral edge web comprises, for example, fabricating the insulating covering layer by means of a spacer technique. To that end, an insulating layer is deposited conformally on the surface and etched back, the insulating covering layer being formed as a lateral edge web in the trench.

A further configuration of the invention provides for the insulating covering layer to have an upper edge, and for the diffusion barrier to be arranged completely below the upper edge. The advantage of this arrangement is cost-effective fabrication. It is a further advantage that if crystal dislocations form at the interface, then they cannot leave the contact region by sliding owing to the dielectric annular layer.

A further configuration of the arrangement according to the invention provides for the covering layer to have an upper

edge and for the conductive contact to be arranged above the upper edge. The advantage of this arrangement is a larger contact area and thus a reduced resistance, particularly when a thin dielectric barrier such as e.g. silicon nitride having a thickness of 1 nm is used.

Furthermore, it is provided that the diffusion barrier is arranged on the conductive contact.

With regard to the method, the object set is achieved by means of a method for fabricating a semiconductor memory cell having the following steps:

- formation of a trench capacitor in a trench, which has an upper region and a lower region and is filled with a conductive trench filling;
- formation of a diffusion barrier on the conductive trench filling;
- epitaxial overgrowth of the diffusion barrier with an epitaxial layer;
- subsequent formation of a selection transistor as a planar transistor above the trench capacitor, a source doping region of the selection transistor being formed in the epitaxial layer.

In one configuration of the method according to the invention, it is provided that after an epitaxial overgrowth of the diffusion barrier, a reflow process is carried out at a higher temperature than the epitaxial overgrowth. The advantage of a reflow process is that the epitaxially grown silicon can planarize a surface due to the elevated temperature for example by means of a flow effect and growth defects are annealed.

A further advantageous configuration of the method according to the invention provides for the reflow process to be carried out with the addition of hydrogen. The advantage of this method step is that an improved planarization and a further reduction of growth defects are achieved.

The dependent claims relate to further advantageous configurations.

The invention is explained in more detail below with reference to exemplary embodiments and figures, in which:

Fig. 1 shows a trench capacitor with a selection transistor;

Fig. 2 shows a further exemplary embodiment of a trench capacitor with a selection transistor;

Fig. 3 shows a further example of a trench capacitor with selection transistor, the trench capacitor being connected to the selection transistor by a conductive contact;

Figs. 4 to 8 show a fabrication method for forming the memory cell illustrated in Fig. 3;

Figs. 9 to 11 show a fabrication method for forming the memory cell illustrated in Fig. 2.

Fig. 1 illustrates a memory cell 1 according to the invention. The memory cell 1 is formed in a substrate 2. The substrate 2 is usually silicon which may be lightly p- or n-doped (10^{15} - 10^{17} dopant atoms per cubic centimeter). The memory cell 1 comprises a trench capacitor 3 and a selection transistor 4. The trench capacitor 3 is formed in a trench 5, the lower region of the trench 5 being surrounded by a buried plate 6.

The buried plate 6 is a conductive layer which may be formed for example by the introduction of dopant into the substrate 2. In accordance with the basic doping of the substrate 2, which may have n- or p-type doping, the buried plate is doped significantly more heavily with up to 10^{21} dopant atoms/cm^3. The buried plate 6 is electrically contact-connected by a buried well 7, which is likewise a doped layer having the same type of dopant as the buried plate 6. An insulation collar 9 is arranged in an upper region of the trench 5. The insulation collar 9 is usually formed from silicon oxide, silicon nitride or a silicon oxynitride. Furthermore, a dielectric layer 8 is formed in the trench 5, which dielectric layer insulates the buried plate 6 in the lower region of the trench 5 and runs on the insulation collar 9 in the upper region of the trench 5. The dielectric layer 8 is formed from a silicon oxynitride, for example. Optionally, a layer stack comprising silicon oxide, silicon nitride and silicon oxynitride may also be involved. The dielectric layer 8 has the task of insulating the buried plate 6 from a conductive trench filling 10 arranged in the trench 5. In this case, the buried plate 6 represents an outer capacitor electrode, the conductive trench filling 10 represents an inner capacitor electrode and the dielectric layer 8 represents the capacitor dielectric.

An isolation trench 11, usually referred to as STI (shallow trench isolation), serves for isolating adjacent memory cells, which are not specifically illustrated in Fig. 1. The selection transistor 4 comprises a source region 12, a drain region 13 and a gate 14, on which a word line 15 is arranged. The source region 12 is connected to a bit line 17 by a bit line contact 16. The bit line 17 is insulated from the word line 15 by means of an intermediate insulation 18. The drain region 13 lies above the trench 5, the drain region 13 being connected to the conductive trench filling 10 by means of a

diffusion barrier 19. The conductive trench filling 10 is usually formed as highly doped and hence low-resistance silicon. In order to prevent the doping of the conductive trench filling 10 from diffusing into the drain region 13 or where possible into the channel of the selection transistor 4, a diffusion barrier 19 is arranged between the conductive trench filling 10 and the drain doping region 13. In this exemplary embodiment, the diffusion barrier 19 is arranged in a planar manner on the conductive trench filling 10. In this case, the diffusion barrier 19 extends from the dielectric layer 8 as far as the isolation trench 11.

Fig. 2 illustrates a further exemplary embodiment of a memory cell 1 according to the invention. The difference from Fig. 1 is that an insulating covering layer 20 with an inner hole 21 is arranged on the conductive trench filling 10. In this exemplary embodiment, the diffusion barrier 19 is arranged in the inner hole 21. By way of example, the insulating covering layer 20 is formed from silicon oxide or silicon nitride or a silicon oxynitride. The diffusion barrier 19 contact-connects the conductive trench filling 10 with the drain doping region 13. Since a part of the cross-sectional area of the trench 5 is covered by the insulating covering layer 20, and only the region of the inner hole 21 and the diffusion barrier 19 are contact-connected by the drain region 13, the drain region 13 and hence the selection transistor 4 can be made significantly smaller. This has the advantage that a larger proportion of the substrate surface can be utilized by the trench capacitor 3 and, and so the capacitance of the trench capacitor 3 can be increased.

A further exemplary embodiment of a memory cell 1 according to the invention is illustrated with reference to Fig. 3. The difference from Fig. 2 is that a conductive contact 22 is

formed in the inner hole 21 arranged in the insulating covering layer 20. For its part, the conductive contact 22 is covered with a diffusion barrier 19, so that the outdiffusion of dopant from the conductive trench filling 10 is prevented by the diffusion barrier 19. The conductive contact 22 is formed in such a way that it projects above an upper edge 27 of the insulating covering layer 20 and thus projects into the drain doping region 13. This ensures a low-resistance contact between the conductive trench filling 10 and the drain region 13.

A method for fabricating the memory cell 1 illustrated in Fig. 3 is described with reference to Figs. 4 to 8. With reference to Fig. 4, a substrate 2 is provided, said substrate being a p-doped silicon substrate, for example. A mask 23 is arranged on the substrate 2, said mask being used to etch the trench 5. The insulation collar 9 is subsequently formed in the upper region of the trench 5 by the customary methods. By introducing dopant into the trench 5, the buried plate 6 is formed in the lower region of the trench 5. Since the substrate 2 is weakly p-doped, a high n-type doping is chosen as doping for the buried plate 6. The buried well 7 may be introduced into the substrate 2 by an implantation, for example, likewise being formed in an n-doped fashion and have an electrical connection to the buried plate 6.

With reference to Fig. 5, the dielectric layer 8 is introduced into the trench 5. By way of example, CVD (chemical vapor deposition) methods and thermal oxidation methods are used for this purpose. By way of example, firstly a thermal oxide layer is formed in the trench 5, which layer is subsequently overgrown with a CVD nitride layer. The conductive trench filling 10 is then formed in the trench 5. The conductive trench filling 10 is formed for example from arsenic- or

phosphorus-doped amorphous silicon or polysilicon. To that end, the doped silicon may be deposited for example by a corresponding CVD method. It is likewise possible for a tungsten, tungsten nitride or tungsten silicide layer to be deposited as conductive trench filling 10 by a CVD method. Since both the dielectric layer 8 and the conductive trench filling 10 are implemented by means of a whole-area deposition process, the dielectric layer 8 and the conductive trench filling 10 are likewise deposited on the mask 23.

With reference to Fig. 6, the conductive trench filling 10 and the dielectric layer 8 are removed from the mask 23 and sunk into the trench 5. In this case, first of all the insulation collar 9 remains and only the dielectric layer 8 and the conductive trench filling 10 are sunk into the trench 5. Afterward, the insulating covering layer 20 is formed in the trench 5 using spacer technology. In this case, the insulating covering layer 20 has an inner hole 21. The conductive contact 22 is deposited into the inner hole 21. In this case, the conductive contact 22 is formed for example from doped polysilicon or amorphous silicon or else a metal such as tungsten or tungsten nitride. In this case, the conductive contact 22 is produced in the inner hole 21 of the insulating covering layer 20. Optionally, by way of example, an insulation layer or a diffusion barrier 19 may be formed on the conductive contact 22.

With reference to Fig. 7, the insulation collar 9 and the insulating covering layer 20 are etched back. This can be carried out for example by means of a timed boron/hydrofluoric acid wet etching or a reactive ion etching using CF_4.

With reference to Fig. 8 a selective silicon epitaxial layer is formed on the uncovered substrate 2 in the trench 5 above

the insulation collar 9. To that end, by way of example, a dry hydrofluoric acid precleaning is carried out. Afterward, at 900°C with the addition of hydrogen with a pressure of 20 torr, the interface area with respect to the substrate 2 can be cleaned of a natural oxide. A selective epitaxy is initiated at 800-1000°C with the addition of silane and hydrogen for an undoped silicon layer, or with the addition of sylane, hydrogen and arsine or phosphine for an in-situ doping of the grown epitaxial layer. It is also suitable firstly to grow an undoped epitaxial layer, to carry out a reflow process and then to grow an epitaxial layer doped in situ with arsenic or phosphorus. The process elements comprising undoped epitaxy, doped epitaxy and reflow process can also be performed a number of times one after the other in corresponding sequences. By means of one or a plurality of reflow processes which are carried out during the selective epitaxy and which are carried out with the addition of hydrogen at 900-1100°C, the surface of the grown epitaxial layer is planarized and possible growth defects in the epitaxial layer are eliminated. In comparison with the conventional epitaxy which can likewise be carried out, this novel process has the advantage that the defect density or the growth defects in the epitaxial layer can be reduced by means of an in-situ hydrogen reflow process at a temperature which is higher than the growth temperature. The reflow process specified can be carried out repeatedly during an epitaxy in order to further reduce the growth defects and in order to adapt the epitaxial layer to arbitrarily complicated topographies in a manner free from defects by means of a repeated sequence of epitaxy and reflow and epitaxy and reflow. Afterward, the epitaxial layer 24 is sunk by means of the mask 23 in order e.g. to terminate with the surface of the substrate 2. This sinking can already be effected during the

reflow process if the thickness of the epitaxial p-type wafer is chosen in accordance with the volume to be filled.

The selection transistor 4 is formed in and on the substrate 2 by conventional methods.

A method variant for fabricating the memory cell illustrated in Fig. 2 is described with reference to Figs. 4, 5, 9, 10 and 11. The fabrication steps which relate to Figs. 4 and 5 are carried out in the manner already described above. Proceeding from Fig. 5, with reference to Fig. 9, the trench 5 is filled with the insulating covering layer 20. This is usually carried out by means of a whole-area CVD process, the insulating covering layer 20 subsequently being removed from the mask 23 by planarization and being sunk into the trench 5 by means of a sinking process, such as reactive ion etching (RIE). In this case, the insulation collar 9 and the dielectric layer 8 are likewise removed from an upper region of the trench 5.

A further method variant proceeding from Fig. 5 is illustrated with reference to Fig. 12. Firstly, the conductive trench filling 10 is sunk into the trench 5. In this case, first of all the insulation collar 9 remains and only the dielectric layer 8 and the conductive trench filling 10 are sunk into the trench 5. Afterward, a thermal nitridation is carried out at temperatures of between 600°C and 1000°C in an ammonia-containing atmosphere, the diffusion barrier 19 being formed with a thickness of between 0.5 nm and 2 nm on the conductive trench filling 10.

With reference to Fig. 13, the insulation collar 9 is etched back. This can be carried out for example by means of a timed boron/hydrofluoric acid wet etching or by means of an

isotropic dry etching by means of reactive ion etching using CF_4.

With reference to Fig. 10, a spacer mask 25 is fabricated by means of spacer technology. The spacer mask 25 is fabricated for example by means of an oxide CVD method and corresponding etching-back steps. In a subsequent RIE (reactive ion etch) etching step, the spacer mask 25 is used to form an inner hole 21 in the insulating covering layer 20. In this case, the inner hole 21 reaches down to the conductive trench filling 10 and uncovers the latter. Afterward, a diffusion barrier 19 made of silicon oxide, silicon nitride, silicon oxynitride with a thickness typically of less than 1.5 nm is formed on the conductive trench filling 10 in the inner hole 21. Conductive layers are formed for example from nitrides or silicides such as tungsten nitride, titanium nitride, tantalum nitride, titanium silicide, cobalt silicide, tungsten silicide or suitable further metals or alloys. A sacrificial layer 26 is subsequently formed in the inner hole 21.

With reference to Fig. 11, first of all the spacer mask 25 is removed by a selective etching process. Afterward, the sacrificial layer 26 is removed likewise in a selective etching step. The substrate 2 is now uncovered in an upper region of the trench 5, so that the insulating covering layer 20 and the diffusion barrier 19 are overgrown with undoped or doped silicon in a subsequent epitaxy step. Since the epitaxially grown silicon grows out of the trench 5 onto the mask 23 during the epitaxial growth process, the grown silicon is planarized to the level of the substrate 2 in a planarization and a sinking step. This is achieved for example by means of an RIE sinking process or by means of a reflow process. In this exemplary embodiment, too, the epitaxial growth of the epitaxial layer 24 can be improved by one or a

plurality of reflow processes carried out in the meantime, thereby reducing growth defects in the epitaxial layer.

Patent claims

1. A semiconductor memory having:
- a trench (5), in which a trench capacitor (3) is arranged;
- a selection transistor (4), which is arranged as a planar transistor above the trench capacitor (3);
- a capacitor dielectric (8), which is arranged in the trench (5);
- a conductive trench filling (10) having a doping as inner capacitor electrode, which is arranged in the trench (5);
- a selection transistor (4) having a drain doping region (13),
characterized in that
- a diffusion barrier (19), which prevents the doping of the conductive trench filling (10) from diffusing into the drain doping region (13), is arranged on the conductive trench filling (10);
- in that an epitaxial layer (24) is grown epitaxially over the diffusion barrier (19), and
- in that the drain doping region (13) of the selection transistor (4) is arranged in the epitaxial layer (24).

2. The semiconductor memory as claimed in claim 1,
characterized in that
the drain doping region (13) of the selection transistor (4) is contact-connected from underneath with the diffusion barrier (19).

3. The semiconductor memory as claimed in either of claims 1 and 2,
characterized in that
the diffusion barrier (19) is arranged horizontally.

4. The arrangement as claimed in one of claims 1 to 3,

characterized in that
an insulating covering layer (20) with an inner hole (21) is arranged on the conductive trench filling (10).

5. The semiconductor memory as claimed in claim 4, characterized in that
a conductive contact (22) is arranged in the inner hole (21).

6. The semiconductor memory as claimed in claim 5, characterized in that
the conductive contact (22) connects the conductive trench filling (10) to the drain doping region (13) of the selection transistor (4).

7. The semiconductor memory as claimed in one of claims 4 to 6,
characterized in that
the cross-sectional area of the inner hole (21) in the insulating covering layer (20) is smaller than the cross-sectional area of the trench (5).

8. The semiconductor memory as claimed in one of claims 4 to 7,
characterized in that
the insulating covering layer (20) is formed as a lateral edge web.

9. The semiconductor memory as claimed in one of claims 4 to 8,
characterized in that
the insulating covering layer (20) has an upper edge (27) and the diffusion barrier (19) is arranged completely below the upper edge (27).

10. The semiconductor memory as claimed in one of claims 4 to 9,
characterized in that
the insulating covering layer (20) has an upper edge (27) and the conductive contact (22) is arranged above the upper edge (27).

11. The semiconductor memory as claimed in one of claims 5 to 8,
characterized in that
the diffusion barrier (19) is arranged on the conductive contact (22).

12. A method for fabricating a semiconductor memory cell having the following steps:
- formation of a trench capacitor (3) in a trench (5), which has an upper region and a lower region and is filled with a conductive trench filling (10) as inner capacitor electrode;
- formation of a selection transistor (4) as a planar transistor with a drain region (13) above the trench capacitor (3),
characterized by
the following further steps:
- formation of a diffusion barrier (19) on the conductive trench filling (10);
- epitaxial overgrowth of the diffusion barrier (19) with an epitaxial layer (24);
the drain region (13) of the selection transistor (4) being formed in the epitaxial layer (24).

13. The method as claimed in claim 12,
characterized in that

after an epitaxial overgrowth of the diffusion barrier (19), a reflow process is carried out at a higher temperature than the epitaxial overgrowth.

14. The method as claimed in claim 13,
characterized in that
the reflow process is carried out with the addition of hydrogen in order to anneal growth defects as a result of flow effects.

15. The method as claimed in either of claims 13 and 14, characterized in that the process sequence comprising epitaxial growth and reflow process is repeated at least once.

Abstract

Semiconductor memory cell with trench capacitor and selection transistor and method for fabricating it.

The present invention relates to a semiconductor memory cell (1), which is formed in a substrate (2) and comprises a trench capacitor (3) and a selection transistor (4). The trench capacitor (3) comprises a capacitor dielectric (8) and a conductive trench filling (10). Arranged on the conductive trench filling (10) is a diffusion barrier (19) on which an epitaxial layer (24) is formed. The selection transistor (4) is arranged as a planar transistor above the trench capacitor (3), a drain doping region (13) of the selection transistor (4) being arranged in the epitaxial layer (24).

Fig. 2

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